Ultra-Low-jitter PLLs for Wireless and Wireline applications

You will explore frequency synthesis for next generation 6G communication and beyond 200Gb/s optical communication

The increasing complexity in future cellular base-stations can be addressed by incorporating direct RF radio transceivers. They are enabled by high performance digital-to-analog converters (DAC) and analog-to-digital converters (ADCs). To enable high data rates (200-Gb/s), the wireline transceivers demand high-performance ADCs and DACs. The Nyquist performance of these data-converters is severely limited by the sampling clock jitter [1]. For example, to achieve 7-b resolution at Nyquist for a 200GS/s data converter the sampling clock jitter needs to be below10fs. The sampling clock for these high-performance data converters must fulfill very stringent in-band and out-of-band spectral mask requirements and should support multiple carrier channels. This demands a sub-10fs jitter phase-locked loop (PLL) with below -80dBc's of spur level.

To achieve below 10fs jitter the power consumption of the PLL can exceed the data converters themselves [1]. This demand calls for fundamental research into a new PLL architecture and innovative circuit implementation to synthesize a low-jitter sampling clock. The CMOS process scaling has increased the DSP power but the performance degradation of RF building blocks used in the PLLs still pose a major bottleneck in achieving the sub-10fs jitter. By considering the limitations of current semiconductor process, the PLL architecture needs to be defined.

During this PhD, the student will be designing a sub-10fs jitter PLL. The starting point will be a literature study and PLL modeling to derive the specifications for the building blocks. Next step would be come up with innovative circuit topologies for key RF building blocks to meet the demanding requirements. Following this will include the layout implementation, post-layout verification and finally measuring the fabricated test chip. This is a challenging PhD topic (also rewarding), requiring a highly motivated PhD student with strong interest in developing design skills.

[1] B. Razavi, "Jitter-Power Trade-Offs in PLLs," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 4, pp. 1381-1387, April 2021, doi: 10.1109/TCSI.2021.3057580.

Required background: Electrical Engineering, IC Design, Circuit Design, Analog and Mixed Signal Design
Type of work: 30% System Modeling, 50% IC Design and Layout, 20% Measurements
Supervisor: Piet Wambacq
Co-supervisor: Jan Craninckx
Daily advisor: Pratap Renukaswamy, Nereo Markulic

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